IN THE CLAIMS

Please amend the claims as follows.

1. (original) A method of forming an LDD of a low temperature polysilicon TFT, comprising:

providing a substrate having a polysilicon layer thereon, wherein the polysilicon layer comprises a first region and a second region;

forming a patterned photoresist layer on the polysilicon layer for exposing the first region and covering the second region, wherein the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, and wherein the middle portion is thicker than the edge portion; and

performing an ion implantation step using the photoresist layer as a mask for simultaneously forming a source/drain in the first region of the polysilicon layer and an LDD in the polysilicon layer underneath the edge portion of the patterned photoresist layer.

2. (original) The method of claim 1, wherein the thickness of the middle portion of the photoresist layer is about 1 to 5 μm and the thickness of the edge portion of the photoresist layer is about 0.1 to 1 μm.

3. (original) The method of claim 1, wherein the width of the LDD is about 0.1 to 1 μm.

4. (original) The method of claim 1, wherein the step of forming the polysilicon layer comprises:

forming an amorphous silicon layer on the substrate;

performing a laser annealing process for transforming the amorphous silicon layer to a polysilicon layer; and

performing a photolithography and etching process for defining the polysilicon layer.

5. (currently amended) The method of claim 1, wherein the ion concentration in the source/drain is about $1x10^{14}$ to $1x10^{15}$ ions/cm^3 ~~ions/cm^2~~, and the ion concentration in the LDD is about $1x10^{12}$ to $1x10^{14}$ ions/cm^3 ~~ions/cm^2~~.

6. (original) A method of forming an LDD of a low temperature polysilicon TFT, comprising:

providing a substrate having a polysilicon layer thereon, wherein the polysilicon layer comprises a first region and a second region;

forming a photoresist layer on the polysilicon layer;

setting a mask above the photoresist layer, wherein the mask comprises a non-exposing region, a exposing region, and a partial-exposing region;

performing a photolithography and etching process for forming a patterned photoresist layer, wherein the first region of the polysilicon layer is exposed and the second region of the polysilicon layer remain covered by the patterned photoresist, wherein the portion of the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, wherein the middle portion is thicker than the edge portion, and wherein the middle portion and the edge portion of the photoresist layer are formed in different thickness through the non-exposing region and the partial-exposing region, respectively; and

performing an ion implantation process by using the patterned photoresist layer as a mask for simultaneously forming a source/drain in the first region of the polysilicon layer and an LDD in the polysilicon layer underneath the edge portion of the patterned photoresist layer.

7. (original) The method of claim 6, wherein the partial-exposing region of the mask comprises a pattern of a plurality of long strips.

8. (original) The method of claim 7, wherein the width of the long strips is about 0.05 to 0.5 μm, and the distance between two adjacent long strips is about 0.05 to 0.5 μm.

9. (original) The method of claim 6, wherein the thickness of the middle portion of the photoresist layer is about 1 to 5 μm, and the thickness of the edge portion of the photoresist layer is about 0.1 to 1 μm.

10. (original) The method of claim 6, wherein the width of the LDD is about 0.1 to 1 μm.

11. (original) The method of claim 6, wherein the step of forming the polysilicon layer comprises:

forming an amorphous silicon layer on the substrate;

performing a laser annealing process for transforming the amorphous silicon layer to a polysilicon layer; and

performing a photolithography and etching process for defining the polysilicon layer.

12. (currently amended) The method of claim 6, wherein the ion concentration in the source/drain is about $1x10^{14}$ to $1x10^{15}$ ions/cm^3 ~~ions/cm^3~~, and the ion concentration in the LDD is about $1x10^{12}$ to $1x10^{14}$ ions/cm^3 ~~ions/cm^3~~.

13. (currently amended) A method of forming an LDD of a semiconductor device, comprising:

providing a substrate comprising a first region and a second region;

forming a photoresist layer on the substrate;

setting a mask above the substrate ~~polysilicon layer~~, wherein the mask comprises a non-exposing region, an exposing region, and a partial-exposing region;

performing a photolithography and etching process for forming a patterned photoresist layer, wherein the first region of the substrate is exposed and the second region of the substrate remain covered by a portion of the patterned photoresist layer, wherein the portion of the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, wherein the middle portion is thicker than the edge portion, and wherein the middle portion and the edge portion of the photoresist layer are formed in different thickness through the non-exposing region and the partial-exposing region; and

performing an ion implantation process using the photoresist layer as a mask for simultaneously forming a source/drain in the first region of the substrate and ~~san~~ an LDD in the substrate underneath the edge portion of the photoresist layer.

14. (original) The method of claim 13, wherein the partial-exposing region of the mask comprises a pattern of a plurality of long strips.

15. (original) The method of claim 14, wherein the width of the long strips is about 0.005 to 0.05 μm, and the distance between two adjacent long strips is about 0.005 to 0.05 μm.

16. (original) The method of claim 13, wherein the thickness of the middle portion of the photoresist layer is about 1 to 5 μm, and the thickness of the edge portion of the photoresist layer is about 0.1 to 1 μm.

17. (original) The method of claim 13, wherein the width of the LDD is about 0.1 to 1 μm.

18. (currently amended) The method of claim 13, wherein the ion concentration in the source/drain is about $1x10^{13}$ to $1x10^{16}$ ions/cm^3 ~~ions/cm^2~~, and the ion concentration in the LDD is about $1x10^{12}$ to $1x10^{15}$ ions/cm^3 ~~ions/cm^2~~.

19. (new) A method of forming a low temperature polysilicon TFT, comprising:

providing a substrate having a polysilicon layer thereon, wherein the polysilicon layer comprises a first region and a second region;

providing a mask comprising a non-exposing region, an exposing region and a partial-exposing region;

forming a patterned photoresist layer on the polysilicon layer for exposing the first region and covering the second region, wherein the patterned photoresist layer covering the second region comprises a middle portion and an edge portion, and wherein the middle portion is thicker than the edge portion;

performing an ion implantation step using the photoresist layer as a mask for simultaneously forming a source/drain in the first region of the polysilicon layer and an LDD in the polysilicon layer underneath the edge portion of the patterned photoresist layer;

removing the patterned photoresist layer;

forming a gate oxide layer over the source/drain and the LDD after forming the source/drain and the LDD; and

forming a gate over the gate oxide layer.

20. (new) A method of forming a low temperature polysilicon TFT, comprising:

providing a substrate having a polysilicon layer thereon, wherein the polysilicon layer comprises a first region and a second region;

forming a photoresist layer on the polysilicon layer;

setting a mask above the photoresist layer, wherein the mask comprises a non-exposing region, a exposing region, and a partial-exposing region;

performing a photolithography and etching process for forming a patterned photoresist layer, wherein the first region of the polysilicon layer is exposed and the second region of the polysilicon layer is covered by the patterned photoresist, wherein a portion of the patterned photoresist layer covering the second region of the polysilicon layer comprises a middle portion and an edge portion, wherein the middle portion is thicker than the edge portion, and wherein the middle portion and the edge portion of the

photoresist layer are formed in different thickness through the non-exposing region and the partial-exposing region, respectively;

performing an ion implantation process by using the patterned photoresist layer as a mask for simultaneously forming a source/drain in the first region of the polysilicon layer and an LDD in the polysilicon layer underneath the edge portion of the patterned photoresist layer;

removing the patterned photoresist layer;

forming a gate oxide layer over the source/drain and the LDD after forming the source/drain and LDD; and

forming a gate over the gate oxide layer.